

# CS Seminar

## ***A Universal Cache Miss Equation for the Memory Hierarchy***

**Professor Y.C. Tay**  
**National University of Singapore**

**Date:**  
**April 6, 2017**  
**Thursday**  
**2:10 pm**

**Venue:**  
**Room 308**  
**Chow Yei Ching Building**  
**The University of Hong Kong**

### **Abstract:**

Where is the science in computer science? To find it, one could start with the observation that, fundamentally, every computation needs resources. This talk focuses on one of them, memory, and describes a multi-year effort to develop one Cache Miss Equation that can be used for different levels of the memory hierarchy. It works for a disk cache, for various application patterns and different operating systems. Its extensions were used to dynamically size the record buffer for a mix of database transactions, the heap for garbage-collected applications (where heap size affects reference pattern), a nonvolatile transcendent memory for virtual machines (where the replacement policy is complicated), and the router partition for Named Data Networking. It also models how two adjacent levels in the memory hierarchy are coupled. Current work is on using the equation to analyze the relationship among miss rates in a cache tree, and how a replacement policy should balance between recency and frequency.

### **About the Speaker:**

Y.C. Tay received his B.Sc. degree from the University of Singapore and Ph.D. degree from Harvard University. He is a professor in the Departments of Mathematics and Computer Science at the National University of Singapore (<http://www.comp.nus.edu.sg/~tayyc>). His main research interest is performance modeling (database transactions, wireless protocols, Internet traffic, memory allocation); other interests include distributed protocols and database systems. He is author of "Analytical Performance Modeling for Computer Systems".

**All are welcome!**  
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