

# CS Seminar

## ***Reevaluating Amdahl's Law in the Multicore Era***

**Prof. Sun Xian-He**  
Department of Computer Science,  
Illinois Institute of Technology

**Date:**  
**June 13, 2009**  
**Saturday**  
**11:00 am**

**Venue:**  
Room 308  
Chow Yei Ching Bldg  
The University of Hong Kong

### **Abstract:**

Multicore architecture has become the trend of high performance processors. While it is generally accepted that we have entered the multicore era, concerns exist on when or will moving into the manycore stage. Recently, Hill and Marty presented a pessimistic view of multicore scalability, citing Amdahl's law and the memory-wall problem. Technology is available, but major vendors are hesitant in making processors that have a large number of cores. This is a very interesting phenomenon, where history seems to repeat itself on the scalability debate of parallel processing that occurred 20 years ago. In this introductory keynote talk we first review the history and concepts of scalable computing, and review the current technologies and the memory-wall problem. We then use the same hardware cost model of multicore chips used by Hill and Marty to introduce two performance models from the scalable computing point of view. These models show that there is no inherent, immovable upper bound on the scalability of multicore architectures. Finally, we conclude with proposed solutions to the memory-wall problem to make the potential scalability of multicore reachable in practice.

### **About the Speaker:**

Dr. Xian-He Sun received his BS in Mathematics in 1982 from Beijing Normal University, P.R. China, and completed his MS in Mathematics, MS and Ph.D. in Computer Science in 1985, 1987, and 1990, respectively, all from Michigan State University. Currently he is a professor at IIT, a guest faculty in the Mathematics and Computer Science Division at the Argonne National Laboratory, a visiting scientist at the Fermi National Accelerator Laboratory, and the director of the Scalable Computing Software laboratory at IIT. His research interests include parallel and distributed processing, middleware, performance evaluation, and high end computing. His memory-bounded (the so-called Sun-Ni's law) and memory access delay performance model are introduced in many modern textbooks as a must known in performance evaluation of scalable computing systems. He received the ONR and ASEE Certificate of Recognition award in 1999, the Best Paper Award at the International Conference on Parallel Processing in 2001, the Best Poster Award at IEEE International SuperComputing Conference in 2003, and the IIT Dean's Excellence Award for Research in 2006. He is a Tan Chin Tuan Fellow, Nanyang Technological University, Singapore, a Guest Professor, University of Science and Technology of China (USTC) and Beijing University of Aeronautics and Astronautic, P. R. China, and the president of the Society of Chinese-American Professors & Scientists.

**All are welcome!**

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